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Reconfigurable Architectures for Wireless Systems: Design Exploration and Integration Challenges

Joseph R. Cavallaro, Michael C. Brogioli, Alexandre de Baynast, and Predrag Radosavljevic,

Center for Multimedia Communication, Department of Electrical and Computer Engineering, Rice University, MS 380, 6100 Main Street, Houston, TX 77005 USA, +1-713-348-4719 (voice), +1-713-348-6196 (fax), cavallar@rice.edu, brogioli@rice.edu, debaynas@ece.rice.edu, rpredrag@rice.edu

***Abstract* — Mobile devices are severely power and area limited due to battery capacity and system size. In many of these example systems, advanced features require computationally complex signal processing on high-speed data streams for enhanced networking capabilities. Thus, mapping high-level communication and networking algorithms to system architectures is a complex and challenging procedure. An important challenge is to characterize the area, time, and power requirements of these embedded system modules and to use this information effectively to determine the architecture of programmable, reconfigurable, and fixed-function modules. In this paper, we will focus on application examples in wireless networking which highlight these challenges in reconfigurable systems integration.**

***Index Terms* — Reconfigurable Elements, Flexible Air-Interface – Physical layer hardware architectures and software environments enabling reconfigurable radio**

Introduction

MOST wireless physical layers are characterized by several signal processing blocks which are similar in their structure and functionality but differ in their implementations. The digital baseband processing complexity is dominated by channel estimation, detection and decoding in the presence of interference. Interconnect is a limited design resource needed for achieving parallelism in these architectures [1-3]. In recent research, we have proposed algorithms and architectures for these three major blocks [4-12, 15, 16] for both base-stations and mobile handsets in cellular and indoor wireless LAN systems. The proposed fixed-function ASIC-like implementations simultaneously achieve high performance and area-power efficiency by exploiting special algorithmic and architectural structures, and it is important to preserve these features when developing reconfigurable systems.

With rapid development and adoption of advanced wireless systems, it is important to reduce the time to develop hardware research prototypes of these new algorithms [17, 18]. It is well known that VLSI implementations consume minimal power but typically require long design cycles. On the other hand, DSPs are completely programmable but are in general unable to meet real-time deadlines and power budgets for high data rate mobile communications. A new class of application specific processors is an area of current research [19]. These architectures are programmable and may also be reconfigurable to allow for application specific instructions [20, 21]. FPGAs present an excellent platform for prototyping and evaluation of these architectures, particularly the class of heterogenous FPGAs that contain both programmable fabric and embedded processor cores. However, there

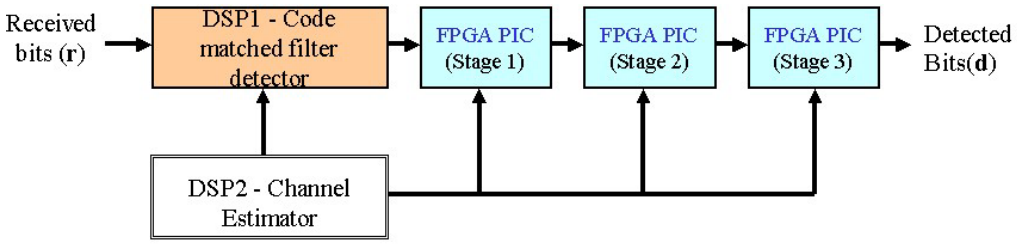

Figure 1: Parallel Interference Cancellation detector example on a hetergeneous DSP-FPGA system. Interconnect among modules may reduce system performance, after [5].

are many new challenges in interconnect design to effectively integrate the embedded host and programmable fabric co-processor functions in these FPGAs, see Figure 1.

Design Exploration and Integration Challenges

Advanced signal processing algorithms contain a number of key numerically intensive kernels. Many of these kernels operate on streams of vectors or matrices and present challenges in interconnect and datapath design. As an example, wireless communication systems are composed of a pipeline of sub-algorithms with varying degrees of instruction and data parallelism. Our key research innovations are in signal processing algorithm to parallel architecture mapping. As wireless systems both increase in data rate and require increased flexibility to adapt to changing environmental channel conditions, VLSI signal processing architectures are expanding from fixed-function ASICs and general programmable DSPs to application-specific instruction processors (ASIPs) and heterogeneous FPGAs with embedded processor cores and programmable fabrics [22-24]. We are investigating the power and interconnect challenges of these systems through partitioning into clusters [25] and the design of host to co-processor interfaces [29]. Our Rice University CMC wireless testbed will contain several high-density Xilinx Virtex-II Pro FPGAs that will allow us to study the efficiency of these devices and to provide FPGA modules and design techniques for intra-chip and inter-chip communication.

As an example, our research in flexible Low Density Parity Check (LDPC) codes [26], has an initial prototype on standard FPGAs. LDPC is a highly parallel algorithm which requires large amounts of interconnect resources, and is therefore a research challenge in system integration. Our use of FPGA systems for rapid prototyping provides new core modules beyond those currently available from existing sources [27,28]. In our current research, we plan to utilize the Rice testbed to verify performance and integration in heterogeneous FPGAs and to make these host to coprocessor interface modules available. Additionally, we will describe our simulation environment for SoC design exploration that models the TI C64x DSP core with customizable programmable co-processors. Our goals are to clearly and carefully model the software and hardware communication interfaces and bottlenecks in heterogeneous systems to improve the modularity and reusability of hardware and software for high data rate reconfigurable communication systems. It is important to model and simulate the data transfer between the hosts and co-processors so that the design of interface port and the communication link reduce the overall system cycle counts. A poorly design interface may actually reduce system performance.

Processor Challenges for 4G Systems

The ongoing definition of 4G wireless systems underscores several urgent challenges for system realization and design. Higher data rates and complex antenna and modulation schemes will require efficient algorithms and flexible chip architectures for baseband processing. Not only will area,

time, and power consumption be the main design constraints, but also system reconfigurability and design reuse will be

1X-EV-DO systems and LDPC decoding has shown the flexibility of these ASIP solutions which will lead to System on Chip (Soc)

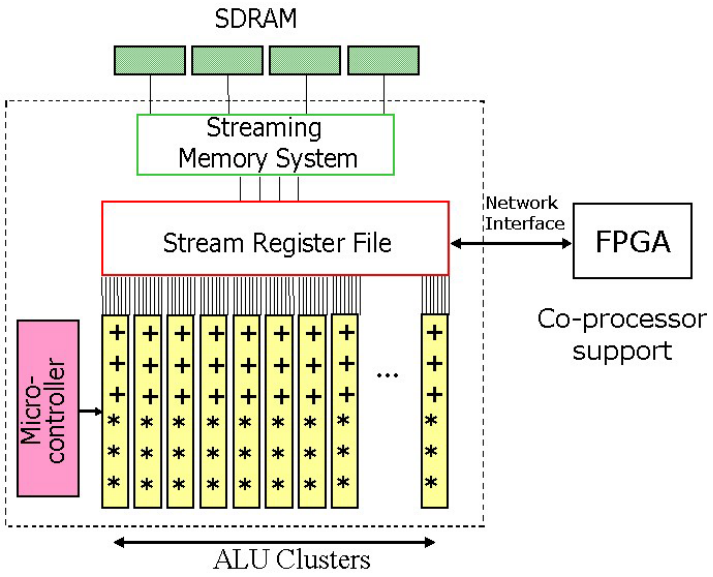

Figure 2: Programmable Multi-cluster Stream processor architecture with FPGA co-processor highlighting interconnect challenges between functional units and register files, after [1].

needed for fast creation of new systems. This flexibility will be key for MIMO antenna processing blocks that may be configured with a varying number of antennas.

As data rates have increased, a single DSP processor is not capable to keep up with the signal processing requirements of advanced algorithms. Multiple DSP processors do not have the power efficiency to exploit the instruction and data parallelism in the algorithms. A solution to this DSP limitation has focused on custom ASIC co-processor designs clustered around a programmable DSP host. However, the multiple co-processor solution requires extensive design and verification time and with the spiraling costs of ASIC fabrication, these systems are increasing in cost and have little ability for re-use or modification. The class of application specific instruction set processors has recently emerged to fill this middle ground between DSP and ASIC solutions. For example, stream processors, as shown in Figure 2, contain multiple SIMD-like clusters with specialized memory systems. Our recent research on chip equalizers for HSDPA and processors. From design exploration of parallelism and flexibility requirements, these future SoC processors will be an efficient integration of DSP, ASIP, and ASIC structures.

For high data rate 4G systems operating at greater than 100 Mbps, there are several research trends that are emerging that will require significant advances in VLSI architectures to provide performance with limited area, time and power constraints. For many MIMO OFDM systems, effective coding will be important. In [30], an iterative turbo-like system integrating LDPC decoding with the receiver is presented. However, for outdoor highly mobile environments, equalization will be needed even in OFDM systems [31,32]. Furthermore, parallel interference cancellation can also be used to enhance these MC-CDMA systems [33]. With the focus in 4G on adapting OFDM, there can also be benefits from applying techniques from WLAN applications, and also from low-power UWB OFDM architectures [34].

In addition to the flexibility needed for

adaptation as 4G standard continue to evolve, there is growing interest in system reconfigurability and design modularization and reuse. However, system reconfigurability typically introduces overhead (lower data rate and higher power) that may not be acceptable in many applications. The commercial aspects of the military XG and JTRS hardware research are leading to cognitive radio and also are studied in the European E2R end to end reconfigurability project and the WWRF WG-6 on Reconfigurability. These current system initiatives highlight research challenges in increasing data rate and lowering power consumption. In order to develop low-cost, low-power systems, there is much research to be done in creating a low-power architecture with an efficient hardware abstraction layer (HAL). This HAL would allow for efficient hardware and software partitioning and for the use of appropriate modules to create an adaptable 4G system. Current wireless system architectural blocks do not have the design standardization and modularization to allow for efficient mix and match for reconfigurable (or cognitive) radio systems. Research in the use of design and architecture simulation tools, such as Xilinx System Generator, are leading to more efficient design reuse strategies.

Conclusion

Reconfigurability and system design and re-use will be important for 4G wireless systems. The mixture of DSP, ASIP, and ASIC structure will require efficient interconnection interfaces for high performance system design. The design of these ports, buffers, queues, and the resulting hardware abstraction layer will need to be optimized for overall system performance. Simulation environments will need to be enhanced to collect system statistics for design exploration of processor utilization and power efficiency.

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